REMARKS

Claims 3-17 are pending in this application of which claims 3, 4, and 9 are independent. Claims 4-15 and 17 have been allowed. Claim 3 has been rejected and claim 16 has been objected to. Claims 16 and 17 have been amended. For the following reasons, this application is in a condition for allowance and should be passed to issue.

Drawing Objections

The Examiner has objected to the drawings under 35 C.F.R. § 1.83(a) alleging that the figures do not illustrate the read and write conversion circuits specified by the claims. To the contrary, the drawings (e.g. Figs. 4, 9, 14, 20, etc.) illustrate a bit-width expansion circuit and a bit-width reduction circuit (or bit-width conversion circuits) corresponding to the read conversion circuit and write conversion circuit of the claims. Though described throughout the application, a brief description of the read and write conversion circuits is provided on page 9, line 24, - page 10, line 1 of the specification. Accordingly, the drawings comply with the requirements under 35 C.F.R. § 1.83(a). Withdrawal of the objection is respectfully solicited.

Claim Rejections

The Examiner rejects claim 3 under 35 U.S.C. § 102(e) as being anticipated by Nishino (U.S. Patent No. 6,366,877). The rejection is traversed.

Nishino discloses an emulation system to overcome problems with an input/output controller (e.g., the Intel 8042 chip) for controlling transmission between a CPU 200 and a keyboard 950 and mouse 960. (See Fig. 2). Nishino addresses various problems associated with the 8042 chip (See col. 1, lines 54-65), and to overcome these,

provides a system for emulating the input/output controller of the 8042 chip without the hardware resource requirements of the 8042 chip. Fig. 3 illustrates one embodiment of the emulation system. Briefly stated, the emulation system comprises a reception/transmission circuit 20, which is configured to perform the reception/transmission of data between reception/transmission circuit 20 and input/output devices including a keyboard 16, a mouse 18, etc. Though described in greater detail (see e.g., col. 8, line 4 - col. 9, line 22), the system of Fig. 3 emulates the operation of the 8042 chip, thereby obviating the need to use the 8042 chip.

For convenient reference, claim 3 is reproduced below.

3.   A semiconductor memory device comprising:

a plurality of input terminals for receiving write data, a control signal and an address signal; and

at least one output terminal, different in number from the input terminal(s) for receiving the write data, for outputting read data, wherein the input terminals are coupled to a first bus, and said at least one output terminal is coupled to a second bus, and each of the first and second buses is a unidirectional bus for transferring a signal or data in one direction.

As to claim 3, the Examiner references Fig. 2 of Nishino illustrating a block diagram of the Intel 8042 chip. The Examiner characterizes the output buffer data bus (line connecting between output buffer 922 and DATA BUS) and the input buffer data bus (line connecting between input buffer 924 and DATA BUS) as the claimed first and second uni-directional data buses. The Examiner also references Fig. 3 of Nishino and alleges that the figure illustrates input terminals different in number than that of the output terminals. In other words, the Examiner asserts output buffer 44 and input buffer 42 of Fig. 3 have terminals different in number and the lines connecting to these buffers

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represent unidirectional data buses for transferring a signal in one direction. The Examiner's interpretation of the reference is flawed in several respects.

First, Nishino fails to teach input or output terminals connected to the input buffer and output buffer. Instead, Nishino merely illustrates various high-level block diagrams of an 8012 processor (Fig. 2) and an emulation system (Fig. 3). A line (the lines between input and output buffers (922, 924) and DATA BUS) connecting to various block components does not necessarily correspond to input and output terminals as the Examiner has suggested. Especially absent any disclosure to the effect, it is not possible to determine any type of terminal configuration corresponding to the buffers of Nishino.

Second, Nishino provides that data is supplied to the input buffer 42; however, there is no disclosure of an input terminal (see supra) or whether the input buffer would receive write data, a control signal and an address signal, as claim 3 recites.

Third, the Examiner alleges that the lines connecting between the buffers of Fig. 2 (and not Fig. 3) and the DATA BUS represent a uni-directional bus, as claim 3 recites. To the contrary, a line with one arrow does not necessarily implicate a uni-directional bus. For example, "DATA BUS" of Fig. 2 is also shown with one arrow, but is in fact bi-directional. If DATA BUS was uni-directional, processor 8042 would be incapable of communicating with the components commonly connected via the bus. Also, Fig. 9 illustrates the structure of the I/O Register 40 whereby the output buffer 42 and input buffer 44 have a single line each connecting to DATA BUS. However, the lines connecting therebetween have an arrow on each end, which may designate a bi-directional bus, and therefore is inconsistent with the Examiner's characterization described above. In light of the inconsistent illustrations and without any further

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description, it would be impermissible to rely solely on the illustrations to show a uni-directional data bus.

Fourth, the Examiner states that "Fig. 3 shows different number of output from input." It is noted that Fig. 2 corresponds to the prior art and Fig. 3 corresponds to an emulation system configured to emulate the processor of Fig. 2. In other words, the Examiner seems to pick pieces from different figures of the reference and alleges that the structure of claim 3 is disclosed. In doing so, the Examiner has ignored the interrelationship of the components of claim 3. That is, the Examiner argues that Fig. 2 illustrates unidirectional buses, and a separate circuit (Fig. 3), which are not related nor combinable with Fig. 2, illustrates input and output terminals different in number. The Examiner's rational is improper.

Also, as to output and input being different in number, the Examiner has not identified any terminals whatsoever in Fig. 3. As understood, since the Examiner characterizes buses connecting to input and output buffers of Fig. 2 as the claimed uni-directional buses, the Examiner could only be referring to the similarly configured input and output buffers 44, 42 of Fig. 3. However, referring to a more detailed configuration of these buffers in Fig. 9, it is explicitly apparent that the input and output buffers have only one line connecting thereto. Following the Examiner's rationale, the input and output terminals are the same in number, contrary to claim 3.
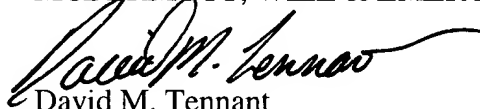
The Examiner's analysis seems to be basically flawed. Nevertheless, the Nishino reference has been thoroughly reviewed, and yet, Nishino fails to teach each and every feature of claim 3. Withdrawal of the rejection is respectfully solicited.

If there are any questions regarding the application or above remarks, the Examiner is encouraged to contact the undersigned in order to expedite prosecution of this case.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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